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Interfacing ISP1161x to Motorola® DragonBall™ EZ RISC Processor

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Application Note
Rev. 2.2

Note: ISP1161x denotes any Philips USB single-chip host and device controller whose name starts with 'ISP1161', this includes ISP1161A, ISP1161A1 and any future derivatives.

Revision History:

Version	Date	Descriptions	Author
2.2	January 2003	• Updated the schematic and Figure 4-1.	Jason Ong
2.1	Aug 2002	• Updated to the latest Philips document template • Changed ISP1161x to ISP1161x • Changed the file name from INTFG_1161_TO_MOTDRAGONBALL-02.pdf.	Kunzang Dolma
2.0	Oct, 2001	Updated schematic to reflect use of ES2	Yuk-lin Ong
1.0	August 2001	First release	Socol Constantin

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Note: ISP1161x denotes any Philips USB single-chip host and device controller whose name starts with 'ISP1161', this includes ISP1161A, ISP1161A1 and any future derivatives.

1. Overview

The unique design of the Philips ISP1161x allows it to be used both as a Host Controller (with two downstream facing ports) and a Device Controller (with one upstream facing port). These ports may be independently accessed, enabling simultaneous connection as a Host Controller and a Device Controller.

When ISP1161x is integrated into a personal digital assistant (PDA) or handheld personal computer (HPC), it is usually connected to the external bus interface of a RISC processor. This application note deals with the critical issues in ISP1161x's embedded design, using the Motorola DragonBall EZ RISC processor as a concrete example.

2. ISP1161x Processor Interface Signals

The processor bus interface of ISP1161x is designed for a simple direct connection with a RISC processor. The data transfer can be done in the Programmed I/O (PIO) or direct memory access (DMA) mode. The estimated maximum data transfer rate on the generic processor bus of ISP1161x is approximately 15 Mbyte/s. This is based on an ISP1161x internal clock frequency value of 48 MHz. To achieve the maximum data transfer rate on the host processor bus, ISP1161x contains a ping pong structured RAM that allows alternative access from the RISC processor or from the internal Host Controller and the Device Controller. The ping pong memory is allocated separately for the Host Controller and the Device Controller. The Host Controller uses 2 kbytes of the ping memory and 2 kbytes of the pong memory in its allocated memory. The Device Controller uses 1.5 kbytes for each of the ping and the pong memory in its own memory.

The main ISP1161x signals to consider for connecting to a Motorola DragonBall EZ RISC processor are:

- A 16-bit data bus (D[15:0]) for ISP1161x., which is "little endian" compatible.
- Two address lines (A0 and A1) necessary for complete addressing of ISP1161x internal registers:
  - **A0 = 0 and A1 = 0**—Selects the Data Port of the Host Controller
  - **A0 = 1 and A1 = 0**—Selects the Command Port of the Host Controller
  - **A0 = 0 and A1 = 1**—Selects the Data Port of the Device Controller
  - **A0 = 1 and A1 = 1**—Selects the Command Port of the Device Controller
- One $\overline{\text{CS}}$ line used to select ISP1161x in a certain address range of the host system. This input signal is active LOW.
- $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are common read and write signals. These signals are active LOW.
- Two DMA channel standard control lines: DREQ1, DREQ2, DACK1, DACK2 and EOT (one channel is used by the Host Controller, and the other channel is used by the Device Controller). Since the DragonBall EZ processor does not contain a DMA controller, these signals will not be used in a minimal hardware implementation.
- Two interrupt lines:
  - INT1 (used by the Host Controller), and
  - INT2 (used by the Device Controller).

  Both have programmable level or edge, and polarity (active HIGH or LOW).
- The CLKOUT signal has a maximum value of 48 MHz.
- The $\overline{\text{RESET}}$ signal is active LOW.

3. Motorola DragonBall EZ

Motorola MC 68EZ328, also called DragonBall EZ, is a processor from the second generation of the DragonBall EZ family. The MC68EZ328 combines a Motorola MC68EC000 processor with intelligent peripheral modules and typical system interface logic. The operating frequency of this processor is 16 MHz, obtained by an internal PLL, which accepts as input a 32.768 kHz crystal, oscillator or a clock signal.

The main internal blocks of the DragonBall-EZ processor to consider when analyzing the bus interface—on which ISP1161x is connected—are:

- The 8-bit or 16-bit 68000-bus interface block.
- The clock synthesizer and power control block.
- The chip-select generation block.
- The interrupt controller.

The DragonBall-EZ processor generates eight programmable general-purpose chip-select signals, which are arranged in four groups of two (CSA[1:0], CSB[1:0], CSC[1:0] and CSD[1:0]). Each chip-select block allows several features to be selected, which may be specific to the devices connected to each selected area:

- Bus size: 8 bits or 16 bits can be independently selected for each area. The default setting corresponds to a 16-bit bus size.
- Number of wait states inserted in a bus cycle can be set from zero to six.
- Each area selected by a CSn can be defined as read-only or read/write access.
- Different types of memory are supported for an area selected by a certain CSn: DRAM, ROM, SRAM and Flash memory.
- The size of any memory area selected by a Chip-Select signal can be selected from a set of predefined ranges (32 kbytes, 64 kbytes, 128 kbytes, 256 kbytes, 512 kbytes, 1 Mbyte, 2 Mbytes and 4 Mbytes).

For a CSn signal to operate correctly, you must program the “Chip-Select Group Base Address Registers” and the “Chip Select Registers”, accordingly.

4. Considerations in Timing Diagrams and WAIT states

The following is a short study of the timing diagrams of ISP1161x.

According to ISP1161x datasheet specifications, a read operation requires the following timing parameters (the requirements of the write operation are similar); see Figure 4-1:

- t_{RL} = 33 ns ($\overline{RD}$ LOW pulse width—minimal value required by ISP1161x),
- t_{RHRL} = 110 ns ($\overline{RD}$ HIGH to next $\overline{RD}$ LOW—minimal value required by ISP1161x) and
- t_{RHDZ} = 3 ns ($\overline{RD}$ hold time, minimal value that can be expected from ISP1161x).
- t_{RC} = 143 ns (will result as a sum of t_{RL} and t_{RHRL})
- t_{SHSL} = 300 ns (first $\overline{RD}$/$\overline{WR}$ after command).

For a detailed analysis of a timing diagram, consider the access of an ISP1161x internal register (for example, the Control Register of the Host Controller). It requires two phases: writing the address (index) of the selected register into the Command Port; then only data transfer access (RD/WR) may take place.

Note: the index of each register is different, depending on whether it is a RD or a WR operation.

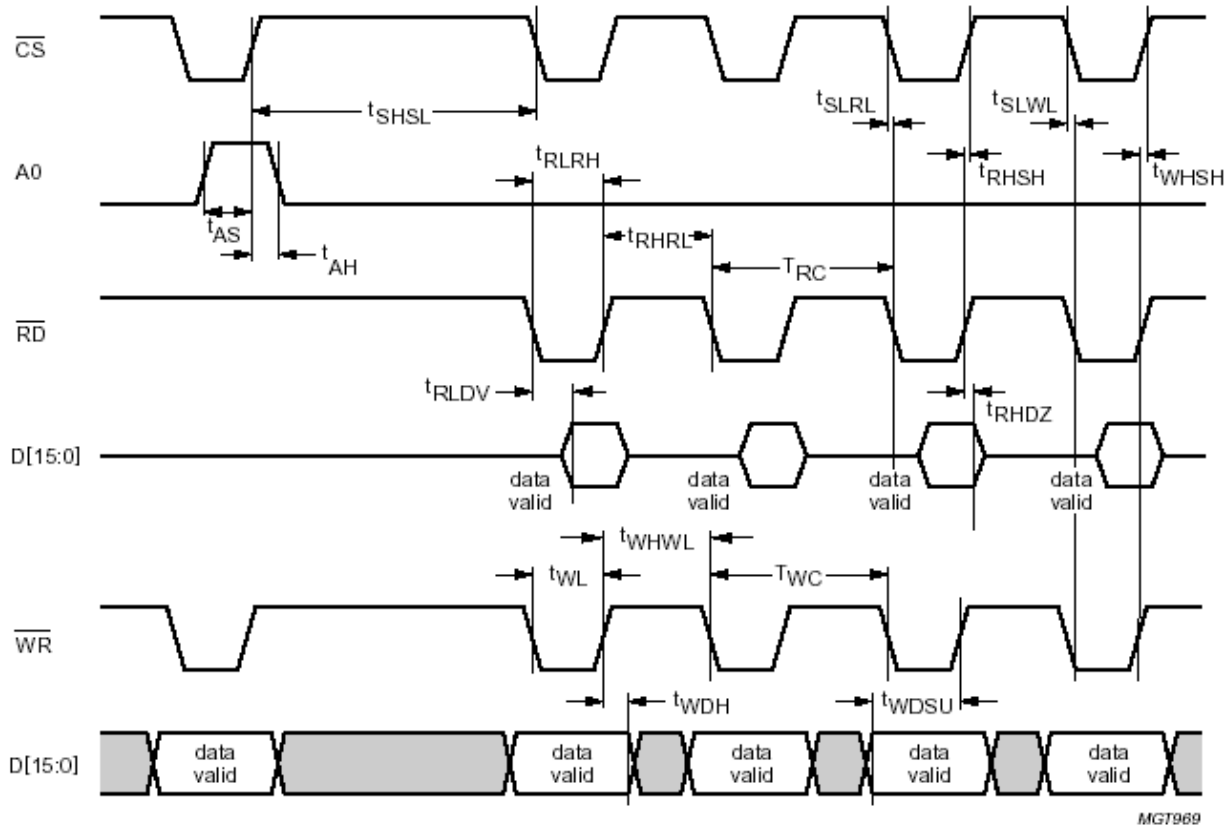


Figure 4-1: Programmed Interface Timing (16-bit Read/Write)

When the ISP1161x connection area is defined as SRAM, ISP1161x will operate correctly for a bus clock CKIO = 33 MHz. Timing measurements show that inserting wait-states in the standard bus cycles of DragonBall EZ is unnecessary. Nevertheless, we will describe wait-state insertion, to cater for cases when faster bus cycles are used for accessing ISP1161x.

Wait states insertion can be implemented through hardware or software. Both solutions will delay the rising edge of $\overline{RD}$ or $\overline{WR}$ to the next CKIO cycle and will determine an elongation of the $\overline{RD}$ or $\overline{WR}$ LOW pulse that can be calculated as:

t_w = W x T(CKIO); where: (W) is the number of wait states desired

T(CKIO) is the cycle length of CKIO.

Note: the value of t_{RHRL} will not be modified by the number of wait states inserted by any of the solutions mentioned earlier. The value of this parameter must be calculated and correctly adjusted according to the number and length of instructions executed by the DragonBall EZ processor between two successive accesses to ISP1161x. The "software solution" for wait-state insertion in a bus cycle is simple and is preferred in a minimal configuration, if additional wait states are necessary.

5. Using Interrupts

ISP1161x will generate two interrupts on the INT1 and INT2 pins, allocated for the Host Controller and the Device Controller, respectively. These interrupts occur depending on the setting of the interrupt registers.

You can connect the INT1 and INT2 signals directly to any of the available IRQ signals of the DragonBall processor. Both INT1 and INT2 of ISP1161x are programmable as active on level or edge and HIGH or LOW, as specified in the *HcHardwareConfiguration Register* and *DcHardwareConfiguration Register* of the Host Controller and the Device Controller, respectively.

6. Suspend and Resume

You can enable ISP1161x to enter the Reset, Resume, Operational and Suspend functional states by programming the *HcControl Register* of the Host Controller or the *DcMode Register* of the Device Controller.

Another way to wake up ISP1161x from the suspend mode is to use the input signals H_WAKEUP (for the Host Controller) and D_WAKEUP (for the Device controller). Monitoring the H_SUSPEND pin (for the host status) and the D_SUSPEND pin (for the device status) can determine the actual status of ISP1161x, without having to access the internal status registers.

ISP1161x may wake up when its $\overline{CS}$ input signal becomes active, if this is desired, by programming a **1** in bit 3 of the *DcHardwareConfiguration Register* of the Device Controller. Alternatively, if the same bit is programmed to a value of **0**, asserting the $\overline{CS}$ signal does not cause ISP1161x to wake up.

7. Schematic Diagram

The schematic diagram on the following page shows the connection of ISP1161x to a Motorola DragonBall EZ processor, in a minimal hardware configuration. For a more detailed description of the connection of ISP1161x to a RISC processor and a study of each category of signals and timing diagrams, refer to the application note *Interfacing ISP1161x to Hitachi SH7709 RISC Processor*.

In this configuration, ISP1161x is selected by CSB0# signal, which is asserted according to the values programmed in the *Chip Select Group Base Address* and *Chip Select Registers* corresponding to CSB0#.

To correctly access ISP1161x, it is assumed that the area selected by CSB0# is programmed for the SRAM memory type and for 16-bit bus width accesses.

Interrupts INT1 and INT2 are connected to the IRQ2 and IRQ3 lines of the DragonBall EZ processor. The interrupt inputs of the DragonBall EZ processor can be set as edge or level sensitive and of positive or negative polarity by programming its *Interrupt Control Register*. ISP1161x also allows programming the polarity (LOW/HIGH) and the signaling mode (level or pulse) for both generated interrupts INT1 and INT2, by setting the bits of the *HcHardwareConfiguration register and the DcHardwareConfiguration register* of the Host Controller and the Device Controller, respectively. This feature of ISP1161x allows a simple connection of the IRQ lines, without any additional logic. The interrupts of the DragonBall processor can be masked in the *Interrupt Mask Register.* Checking the status of an interrupt line can be done by monitoring the values of the *Interrupt Status Register* and the *Interrupt Pending Register* of the DragonBall-EZ processor.

Analysis of the timing diagrams of ISP1161x and the DragonBall-EZ processor, running at a standard frequency of 16 MHz, shows that inserting wait states in a standard bus cycle is unnecessary. In case a similar RISC processor with a higher bus frequency is used, you can insert a certain number of wait-states during a bus cycle (accessing a certain system resource selected by CSn) by programming the selected value of wait states in the corresponding *(Chip-Select) n Register* of the DragonBall processor.

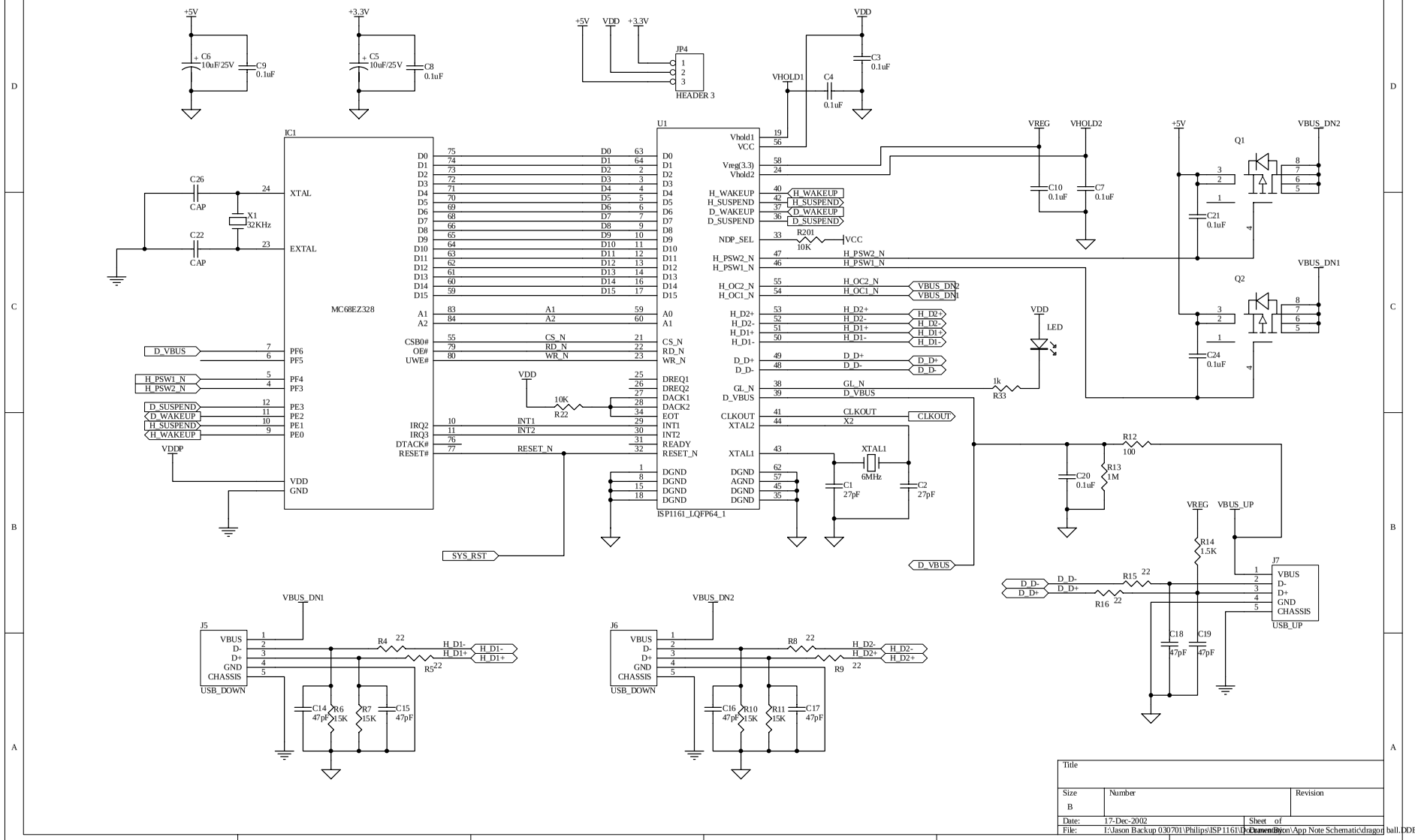
Input signals $\overline{\text{H\_OC1}}$ and $\overline{\text{H\_OC2}}$ are used by ISP1161x to detect an overcurrent on the downstream ports. Since separate overcurrent detection and protection circuits are implemented in ISP1161x, detection of an overcurrent on a downstream port will have power off at that port only. Connecting the voltages of the two downstream ports VBUS_DN1 and VBUS_DN2 to the $\overline{\text{H\_OC1}}$ and $\overline{\text{H\_OC2}}$ pins enable detection of the current value by sensing the voltage drop on Q1 and Q2 which are MOSFET transistors with very low switch-on resistance Rds. Selection between Q1 and Q2 depends on the desired maximum current value and this determines the value of Rds(on). For example, if a voltage drop of 75 mV will trigger the overcurrent circuitry and the allowed maximum current is about 0.5 A, Rds (on) of approximately 150 MΩ will result. Connecting the ISP1161x input pins $\overline{\text{H\_OC1}}$ and $\overline{\text{H\_OC2}}$ to +5 V will disable ISP1161x's internal overcurrent protection. You can opt for an external overcurrent protection circuit.

The number of downstream ports is determined by the setting of the NDP_SEL input signal of ISP1161x. In a minimal hardware configuration, you can use a simple jumper option to set one or two downstream ports accordingly.

Detection of a connection on the upstream port is achieved by connecting VBUS_UP to pin D_VBUS of ISP1161x. R12 and C20 will act as a low-pass filter that eliminates the possibility of sensing false voltage drop due to load current variations or noise on VBUS_UP. It is recommended, if possible, to implement a hybrid power solution, by using VBUS_UP to provide power to ISP1161x and an external power source for the rest of the system.

The GoodLink™ ($\overline{\text{GL}}$) output signal indicates (using an LED) the status of the USB device and helps in troubleshooting the USB connection.

The $\overline{\text{RESET}}$ input signal of ISP1161x is connected to the system RESET signal, which also generates the RESET# input signal for the DragonBall-EZ processor.


+5V
+3.3V
C6
10uF/25V
C9
0.1uF
C5
10uF/25V
C8
0.1uF
JP4
HEADER 3
VDD
C3
0.1uF
VHOLD1
C4
0.1uF
IC1
MC68EZ328
XTAL
EXTAL
C26
CAP
C22
CAP
X1
32KHz
U1
ISP1161_LQFP64_1
VREG
VHOLD2
C10
0.1uF
C7
0.1uF
Q1
Q2
C21
0.1uF
C24
0.1uF
VBUS_DN2
VBUS_DN1
LED
R33
1k
R12
100
R13
1M
C20
0.1uF
XTAL1
6MHz
C1
27pF
C2
27pF
R201
10K
R22
10K
SYS_RST
D_VBUS
CLKOUT
H_WAKEUP
H_SUSPEND
D_WAKEUP
D_SUSPEND
H_PSW1_N
H_PSW2_N
H_OC1_N
H_OC2_N
H_D1+
H_D1-
H_D2+
H_D2-
D_D+
D_D-
GL_N
NDP_SEL
VBUS_UP
R14
1.5K
R15
22
R16
22
J7
USB_UP
J5
USB_DOWN
J6
USB_DOWN
R4
22
R5
22
R8
22
R9
22
C14
47pF
R6
15K
R7
15K
C15
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C16
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R11
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I:\Jason Backup 030701\Philips\ISP1161\Documentation\App Note Schematic\dragon ball.DDB

8. References

- *Universal Serial Bus Specification Rev. 2.0*
- *ISP1161A1 Full-speed Universal Serial Bus single-chip host and device controller* datasheet
- *ISP1161A Full-speed Universal Serial Bus single-chip host and device controller* datasheet
- *ISP1161 Full-speed Universal Serial Bus single-chip host and device controller datasheet*
- *Interfacing ISP1161x to Hitachi SH7709 RISC Processor* application note

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